UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,030	03/27/2006	Robertus Theodorus Franciscus Van Schaijk	NL03 1167 US1	8030

65913 7590 07/29/2008

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
HSIEH, HSIN YI	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
07/29/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/574,030	VAN SCHAIJK ET AL.	
	Examiner	Art Unit	
	Hsin-Yi (Steven) Hsieh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/17/2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8,10,11 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,10,11 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 1, 3-8, 10, 11, and 13** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. **Claims 1, 8, and 11** recite the limitation "oxygen diffusion through the dielectric material" to characterize the dielectric material in the 12th line of the claim 1, the 6th line of claim 8, and the 7th line of claim 11. The recitation "oxygen diffusion through the dielectric material" is a process which depends on the oxygen content of the environment, and the thickness of dielectric material, which is not related to the property of the material. It is recommend changing it to "oxygen diffusion coefficient of the dielectric material" or similar physical parameters related to the dielectric material.

4. **Claim 10** recites the limitation "a spacer" in the third line of the claim. It is unclear whether this limitation is the same as the "spacers" recited in the last line of claim 8, which claim 10 depends on. If the limitations are the same, please use "the spacer" instead of "a spacer". If the limitations are different, please use a different term, e.g. "a first spacer".

5. **Claims 3-7 and 13** are rejected because they depend on the rejected claims 1 and 11.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. **Claims 1, 3-5, 7, 8, 10, 11, and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US 5,991,204 A) and in view of Sharma et al. (US 5,488,579 A).

9. Chang teaches, regarding to **claim 1**, a method of manufacturing on a substrate (semiconductor substrate 100; Fig. 1a, col. 3 line 58) a 2-transistor memory cell (Flash EEPROM cell; Abstract) comprising a storage transistor (the transistor formed under 101) having a memory gate stack (the gate stack under 101) and a selecting transistor (the transistor under 107), there being a tunnel dielectric layer (floating gate oxide layer 104; Fig. 1a, col. 4 lines 2-3) between the substrate (100) and the memory gate stack (the gate stack under 101), the method comprising: forming the memory gate stack (the gate stack under 101) by providing a first conductive layer (floating gate poly 103 in Fig. 6a before the etching) and a second conductive

layer (second poly; col. 8 lines 55-58) and etching the second conductive layer (second poly) thus forming a control gate (101; Fig. 6a, col. 8 lines 55-58) and etching the first conductive layer (floating gate poly 103 in Fig. 6a before the etching) thus forming a floating gate (floating gate poly 103 in Fig. 6b, col. 8 lines 62-65), the method furthermore comprising, before etching the first conductive layer (floating gate poly 103 in Fig. 6a before the etching), forming spacers (control gate spacer 106; Fig. 6a, col. 8 lines 62-65) against the control gate (101) in the direction of a channel (active channel region 113; Fig. 1a, col. 3 line 62; the direction of channel is the direction from the source to drain) to be formed under the tunnel dielectric layer (104; see Fig. 1a), and thereafter using the spacers (106) as a hard mask (col. 8 lines 62-65) to etch the first conductive layer (floating gate poly 103 in Fig. 6a before the etching) thus forming the floating gate (floating gate poly 103 in Fig. 6b after the etching), regarding to **claim 8**, a 2-transistor memory cell (Flash EEPROM cell; Abstract) comprising, a storage transistor (the transistor formed under 101) and a selecting transistor (the transistor under 107), the storage transistor (the transistor formed under 101) comprising a floating gate (floating gate poly 103 in Fig. 6b, col. 8 lines 62-65) and a control gate (101; Fig. 6a, col. 8 lines 55-58), wherein the control gate is smaller than the floating gate (control gate is shorted than the floating gate; see Fig. 1a), spacers (control gate spacer 106; Fig. 6a, col. 8 lines 62-65) are present next to the control gate (101; see Fig. 1a), and regarding to **claim 11**, an electronic device (Flash EEPROM arrays; col. 3 lines 54-55) comprising a 2-transistor memory cell (Flash EEPROM cell; Abstract), the 2-transistor memory cell including, a storage transistor (the transistor formed under 101) and a selecting transistor (the transistor under 107), the storage transistor comprising a floating gate (floating gate poly 103 in Fig. 6b, col. 8 lines 62-65) and a control gate (101; Fig. 6a, col. 8 lines 55-58),

wherein the control gate is smaller than the floating gate (control gate is shorted than the floating gate; see Fig. 1a), spacers (control gate spacer 106; Fig. 6a, col. 8 lines 62-65) are present next to the control gate (101; see Fig. 1a).

Chang does not teach, regarding to **claim 1**, the spacers being formed from a dielectric material having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers, regarding to **claim 3**, the dielectric material having an oxygen diffusion through the material that is an order of magnitude smaller than oxygen diffusion through oxide spacers includes one or more of silicon nitride, silicon carbide or meal oxide, regarding to **claim 8**, the spacers are made from a dielectric material having an oxygen diffusion through the dielectric material that is an order of magnitude smaller than oxygen diffusion through oxide spacers, and regarding to **claim 11**, the spacers are made from a dielectric material having an oxygen diffusion through the dielectric material that, relative to oxide spacers, is an order of magnitude smaller than the oxygen diffusion through oxide spacers.

In the same field of nonvolatile memory, Sharma et al. teach , regarding to **claim 1**, the spacers (nitride sidewall spacer 37; Fig. 2, col. 4 line 52) being formed from a dielectric material (silicon nitride) having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers (silicon nitride has the oxygen diffusion an order of magnitude small than that of the oxide), regarding to **claim 3**, the dielectric material (silicon nitride; col. 4 line 52) having an oxygen diffusion through the material that is an order of magnitude smaller than oxygen diffusion through oxide spacers includes one or more of silicon nitride, silicon carbide or meal oxide

(silicon nitride), regarding to **claim 8**, the spacers (nitride sidewall spacer 37; Fig. 2, col. 4 line 52) are made from a dielectric material (silicon nitride) having an oxygen diffusion through the dielectric material that is an order of magnitude smaller than oxygen diffusion through oxide spacers (silicon nitride has the oxygen diffusion an order of magnitude small than that of the oxide), and regarding to **claim 11**, the spacers (nitride sidewall spacer 37; Fig. 2, col. 4 line 52) are made from a dielectric material (silicon nitride) having an oxygen diffusion through the dielectric material that, relative to oxide spacers, is an order of magnitude smaller than the oxygen diffusion through oxide spacers (silicon nitride has the oxygen diffusion an order of magnitude small than that of the oxide).

Sharma et al. also teach that the nitride spacer smoothes the topography created by the polysilicon gate and eliminates any sharp corners or edges of polysilicon gate from protruding into overlying layers (col. 4 lines 55-58).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Chang and Sharma et al. using the nitride spacers as taught by Sharma et al., because the nitride spacer smoothes the topography created by the polysilicon gate and eliminates any sharp corners or edges of polysilicon gate from protruding into overlying layers as taught by Sharma et al.

10. Regarding **claim 4**, Chang also teaches a method according to claim 1, furthermore comprising, before forming the memory gate stack, applying the tunnel dielectric layer (104) on the substrate (100; this is shown in Fig. 6a), and after formation of the memory gate stack (see Fig. 6b), removing the tunnel dielectric layer (104) by a selective etching technique (stripping, col. 9 lines 1-2) at least at a location where the selecting transistor is to be formed (all the

exposed area including the selecting transistor region; col. 9 lines 1-2), the selective etching technique preferentially etching the tunnel dielectric layer compared to the substrate ("stripping" indicates only removing the tunnel dielectric layer without removing the substrate).

11. Regarding **claim 5**, Chang also teaches a method according to claim 1, comprising, after etching of the first conductive layer (floating gate poly 103 in Fig. 6a before the etching), providing a floating gate dielectric (poly tunnel oxide 109; Fig. 6c, col. 9 lines 3-6) next to the formed floating gate (103) and at the same time providing an access gate dielectric (erased gate oxide 112; Fig. 6c, col. 9 lines 3-6).

12. Regarding **claim 7**, Chang also teaches a method according to claim 1, the selecting transistor (the transistor under 107) comprising an access gate (erase gate 107; Fig. 6c, col. 4 line 7), the method comprising forming the access gate (107) while the spacer (106) at the access gate (107) side is still present (see Fig. 6c).

13. Regarding **claim 10**, Chang also teaches a memory cell according to claim 8, the selecting transistor (the transistor under 107) comprising an access gate (erase gate 107; Fig. 6c, col. 4 line 7), a spacer (control gate spacer 106; Fig. 6a, col. 8 lines 62-65) being present between the control gate (101) and the access gate (107) and a floating gate dielectric (poly tunnel oxide 109; Fig. 6c, col. 9 lines 3-6) being present between the floating gate (103) and the access gate (107), wherein the spacer (106) is thicker than the floating gate dielectric (109; see Fig. 1a).

14. Regarding **claim 13**, Chang also teaches the selecting transistor (the transistor under 107) includes, an access gate (erase gate 107; Fig. 6c, col. 4 line 7), a spacer (control gate spacer 106; Fig. 6a, col. 8 lines 62-65) being present between the control gate (101), and the access gate (107) and a floating gate dielectric (poly tunnel oxide 109; Fig. 6c, col. 9 lines 3-6) being present

between the floating gate (103) and the access gate (107), wherein the spacer (106) is thicker than the floating gate dielectric (109; see Fig. 1a).

15. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang and Sharma as applied to claim 1 above, and further in view of Chen (US 6,091,104 A).

Regarding **claim 6**, Chang teaches a method according to claim 1, the memory gate stack (the gate stack under 101) comprising an interlayer dielectric layer (a layer 102 of oxide/nitride/oxide (ONO); Fig. 1a, col. 3 lines 64-65) between the first conductive layer (103) and the second conductive layer (102), the method furthermore comprising removing part of the interlayer dielectric layer (102) before forming the spacers (this can be shown in Fig. 6a and Fig. 6b, where 102 is left only under the control gate 101 and is enclosed by the spacer 106).

Chang does not teach removing part of the interlayer dielectric layer after forming the control gate.

In the same field of nonvolatile memory, Chen teaches removing part of the interlayer dielectric layer after forming the control gate (col. 4 lines 64-67). Chen also teaches that the control gate is used as mask that only one lithographical mask is needed to form the gate stack (col. 4 lines 44-67).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Chang and Chen and remove the interlayer dielectric layer after forming the control gate as taught by Chen, because only one lithographical mask is needed to form the gate stack as taught by Chen.

Response to Arguments

16. Applicant's arguments with respect to claims 1, 8, and 11 have been considered but are moot in view of the new ground(s) of rejection.

17. Applicant's amendments, filed 03/17/2008, overcome the objections to the drawings and the rejections to claims 2-3, 9 and 12-13 under 35 U.S.C. 112. The objections to the drawings and the rejections to claims 2-3, 9 and 12-13 have been withdrawn. The rejection to claim 10 still stands because the referring of the limitation "a spacer" to two different elements is indefinite.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsin-Yi (Steven) Hsieh whose telephone number is 571-270-3043. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/H. H./
Examiner, Art Unit 2811
7/19/2008